

1 WHAT IS CLAIMED IS

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1. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate

10 adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

15 forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

20 forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

25 said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

25 depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

30 forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

35 removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

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1 removing said first insulation film exposed
at a bottom of said contact hole selectively with
respect to said diffusion region;

5 wherein said step of forming said first
insulation film is conducted by a plasma CVD process,
with a high-frequency power set smaller than a high-
frequency power in which said first insulation film
contains H₂O with an amount of about 2.4 wt%.

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15 2. A method as claimed in claim 1, wherein
said high-frequency power is set smaller than a high-
frequency power in which said first insulation film
contains H₂O with an about of about 1.1 wt% or less.

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3. A method as claimed in claim 1, wherein
said high-frequency power is set smaller than about
100 W.

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30 4. A method as claimed in claim 1, wherein
said high-frequency power is set between about 50 W
and about 100 W.

35 5. A method as claimed in claim 1, wherein
said first insulation film has a refractive index of
about 1.5.

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1 6. A method as claimed in claim 1, wherein
said plasma CVD process is conducted while using SiH₄
and N₂O as source materials, with a proportion of N₂O
with respect to SiH₄ set to be about 10 or less.

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10 7. A method as claimed in claim 1, further
including a step, after said step of forming said
first insulation film and before said step of forming
said second insulation film, of annealing said first
insulation film.

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20 8. A method as claimed in claim 7, wherein
said annealing step is conducted by a rapid heating
process.

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25 9. A method as claimed in claim 1, wherein
said step of forming said first insulation film and
said step of forming said second insulation film are
conducted in a common reaction vessel, without a step
of taking out said substrate outside said reaction
30 vessel.

35 10. A method as claimed in claim 1,
wherein said step of forming said diffusion region
includes a step of forming a silicide on a surface of

1 said diffusion region, and wherein said step of
2 forming said silicide is conducted before said step of
3 forming said first insulation film.

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10 11. A method as claimed in claim 1, further
comprising a step, before said step of forming said
11 first insulation layer, of forming a conductor pattern
in contact with said diffusion region.

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12. A method of fabricating a semiconductor
device, comprising the steps of:
13 forming a gate electrode on a substrate;
14 forming a diffusion region in said substrate
15 adjacent to said gate electrode;
16 forming a side wall oxide film on a side
17 wall of said gate electrode;
18 forming an interlayer insulation film on
19 said substrate such that said interlayer insulation
20 film covers said gate electrode and further said side
21 wall oxide film; and
22 forming a self-aligned opening in said
23 interlayer insulation film such that said self-aligned
24 opening exposes said diffusion region;
25 said step of forming said self-aligned
26 opening comprising the steps of:
27 forming a first insulation film of an oxide
28 such that said first insulation film covers said side
29 wall oxide film and said diffusion region;
30 depositing a second insulation film having a
31 composition different from a composition of said first
32 insulation film, on said first insulation film;

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- 1 forming said interlayer insulation film on
said second insulation film;
- 5 forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
region by an etching process while using said second
insulation film as an etching stopper;
- 10 removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
stopper; and
- 15 removing said first insulation film exposed
at a bottom of said contact hole selectively with
respect to said diffusion region;
- 20 wherein said step of forming said first
insulation film is conducted by a CVD process that
uses SiH₄ and N₂O as source gases.

20 13. A method as claimed in claim 12,
wherein said CVD process is conducted while setting a
ratio of N_2O with respect to SiH_4 to about 5 or less.

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14. A method as claimed in claim 12,
wherein said CVD process is conducted at a substrate
30 temperature of about 825°C or less.

35 15. A method as claimed in claim 12,
further including a step, after said step of forming
said first insulation film and before said step of

1 forming said second insulation film, of annealing said
first insulation film.

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16. A method as claimed in claim 12,
wherein said annealing step is conducted by a rapid
heating process.

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15 17. A method as claimed in claim 12,
wherein said step of forming said first insulation
film and said step of forming said second insulation
film are conducted in a common reaction vessel,
without a step of taking out said substrate outside
said reaction vessel.

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25 18. A method as claimed in claim 12,
wherein said step of forming said diffusion region
includes a step of forming a silicide on a surface of
said diffusion region, and wherein said step of
forming said silicide is conducted before said step of
forming said first insulation film.

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35 19. A method of fabricating a semiconductor
device, comprising the steps of:
 forming a gate electrode on a substrate;
 forming a diffusion region in said substrate

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1 adjacent to said gate electrode;
2 forming a side wall oxide film on a side
3 wall of said gate electrode;
4 forming an interlayer insulation film on
5 said substrate such that said interlayer insulation
6 film covers said gate electrode and further said side
7 wall oxide film; and
8 forming a self-aligned opening in said
9 interlayer insulation film such that said self-aligned
10 opening exposes said diffusion region;
11 said step of forming said self-aligned
12 opening comprising the steps of:
13 forming a first insulation film of an oxide
14 such that said first insulation film covers said side
15 wall oxide film and said diffusion region;
16 depositing a second insulation film having a
17 composition different from a composition of said first
18 insulation film, on said first insulation film;
19 forming said interlayer insulation film on
20 said second insulation film;
21 forming a contact hole in said interlayer
22 insulation film in correspondence to said diffusion
23 region by an etching process while using said second
24 insulation film as an etching stopper;
25 removing said second insulation film exposed
26 at a bottom of said contact hole by an etching process
27 while using said first insulation film as an etching
28 stopper; and
29 removing said first insulation film exposed
30 at a bottom of said contact hole selectively with
respect to said diffusion region;
31 wherein said step of forming said first
32 insulation film is conducted by depositing a silicate
33 glass containing P.

1 20. A method as claimed in claim 19,
wherein said silicate glass contains P therein with an
amount of about 6 wt% or less.

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21. A method as claimed in claim 19,
wherein said silicate glass further contains B.

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22. A method as claimed in claim 21,
15 wherein said silicate glass contains B with an amount
of about 4 wt% or less.

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23. A method as claimed in claim 19,
further including a step, after said step of forming
said first insulation film and before said step of
forming said second insulation film, of annealing said
25 first insulation film.

30 24. A method as claimed in claim 23,
wherein said annealing step is conducted by a rapid
heating process.

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25. A method as claimed in claim 19,

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1 wherein said step of forming said first insulation
 film and said step of forming said second insulation
 film are conducted in a common reaction vessel,
 without a step of taking out said substrate outside
5 said reaction vessel.

10 26. A method as claimed in claim 19,
 wherein said step of forming said diffusion region
 includes a step of forming a silicide on a surface of
 said diffusion region, and wherein said step of
 forming said silicide is conducted before said step of
15 forming said first insulation film.

20 27. A method as claimed in claim 19,
 further comprising a step, before said step of forming
 said first insulation layer, of forming a conductor
 pattern in contact with said diffusion region.

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30 28. A semiconductor device, comprising:
 a substrate;
 a gate electrode provided on said substrate;
 a diffusion region formed in said substrate
 adjacent to said gate electrode;
 a side-wall insulation film formed on a side
 wall of said gate electrode; and
35 a self-aligned contact hole defined by said
 side-wall oxide film and exposing said diffusion
 region;

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1 wherein said semiconductor device further
includes:

5 a first insulation film provided on said
gate electrode so as to cover said side wall oxide
film partially;

10 a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
film;

15 an interlayer insulation film deposited on
said second insulation film;

20 a contact hole formed in said interlayer
insulation film, said contact hole extending through
said first and second insulation films and exposing
said self-aligned contact hole;

25 said first insulation film contains H_2O with
an amount, smaller than about 2.4 wt%.

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25 29. A semiconductor device as claimed in
claim 28, wherein said first insulation film contains
 H_2O with an amount of about 1.1 wt% or less.

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35 30. A semiconductor device as claimed in
claim 28, wherein said first insulation film is an
oxide film having a refractive index of about 1.5.

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36 31. A semiconductor device as claimed in
claim 28, further comprising a conductor pattern

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1 contacting with said diffusion region and said gate
electrode such that said conductor pattern extends
between said side wall oxide film and said first
insulation film along a surface of said side wall
5 oxide film.

10 32. A semiconductor device as claimed in
claim 28, further comprising a silicide layer on a
surface of said diffusion region.

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33. A semiconductor device as claimed in
claim 32, further comprising a silicide layer on a
surface of said gate electrode.

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34. A semiconductor device, comprising:
a substrate;
a gate electrode provided on said substrate;
a diffusion region formed in said substrate
adjacent to said gate electrode;
a side-wall insulation film formed on a side
30 wall of said gate electrode; and
a self-aligned contact hole defined by said
side-wall oxide film and exposing said diffusion
region;
wherein said semiconductor device further
35 includes:
a first insulation film provided on said
gate electrode so as to cover said side wall oxide

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1 film partially;
a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
5 film;
an interlayer insulation film deposited on
said second insulation film;
a contact hole formed in said interlayer
insulation film, said contact hole extending through
10 said first and second insulation films and exposing
said self-aligned contact hole;
said first insulation film is formed of PSG
containing P with an amount of about 6 wt% or less.

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35. A semiconductor device as claimed in
claim 34, further comprising a conductor pattern
20 contacting with said diffusion region and said gate
electrode such that said conductor pattern extends
between said side wall oxide film and said first
insulation film along a surface of said side wall
oxide film.

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36. A semiconductor device as claimed in
30 claim 34, further comprising a silicide layer on a
surface of said diffusion region.

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38. A semiconductor device as claimed in
claim 36, further comprising a silicide layer on a

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1 surface of said gate electrode.

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39. A semiconductor device, comprising:
a substrate;
a gate electrode provided on said substrate;
a diffusion region formed in said substrate
10 adjacent to said gate electrode;

a side-wall insulation film formed on a side
wall of said gate electrode; and
a self-aligned contact hole defined by said
side-wall oxide film and exposing said diffusion
15 region;

wherein said semiconductor device further
includes:

20 a first insulation film provided on said
gate electrode so as to cover said side wall oxide
film partially;

a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
film;

25 an interlayer insulation film deposited on
said second insulation film;

a contact hole formed in said interlayer
insulation film, said contact hole extending through
said first and second insulation films and exposing
30 said self-aligned contact hole;

said first insulation film is formed of BPSG
containing B with an amount of about 4 wt% or less.

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A 40. A semiconductor device as claimed in

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1 claim 39, further comprising a conductor pattern
38 contacting with said diffusion region and said gate
electrode such that said conductor pattern extends
between said side wall oxide film and said first
5 insulation film along a surface of said side wall
oxide film.

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41. A semiconductor device as claimed in
claim 39, further comprising a silicide layer on a
surface of said diffusion region.

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42. A semiconductor device as claimed in
claim 41, further comprising a silicide layer on a
surface of said gate electrode.

Claims
were renumbered.
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New renumbered
claim numbers.
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